1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of ROM, and 192 bytes of static RAM.

2. Features

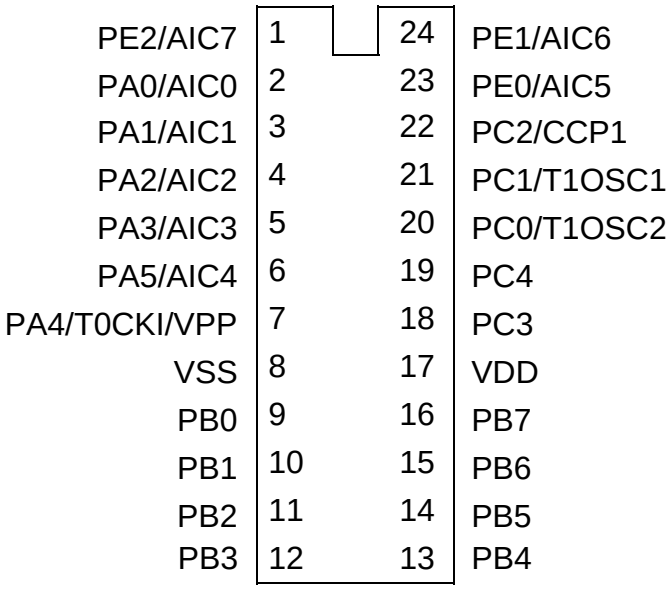
The followings are some of the features on the hardware and software:

- Fully CMOS static design
- 8-bit data bus
- On chip EPROM size: 4.0 K words
- Internal RAM size: 192 bytes
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage: 2.5 V ~ 5.5 V (PRD Disable)
  4.5 V ~ 5.5 V (PRD Enable)
- Operating frequency: DC ~ 20 MHz
- The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Power edge-detector Reset
- Power range-detector Reset
- Sleep Mode for power saving
- Capture, Compare, PWM module
- 7 interrupt sources:
  -External INT pin
  -TMR0 timer, TMR1 timer, TMR2 timer
  -A/D conversion completion
  -Port B<7:4> interrupt on change
  -CCP1
- A/D converter module:
  -8 analog inputs multiplexed into one A/D converter
  -10-bit resolution
- TMR0: 8-bit real time clock/counter
  TMR1: 16-bit real time clock/count
  TMR2: 8-bit clock/counter (internal)
- 5 types of oscillator can be selected by programming option:
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
  IRC－Internal 8MHz RC oscillator
- On-chip RC oscillator based Watchdog Timer (WDT)
- 18/20 I/O pins with their own independent direction control

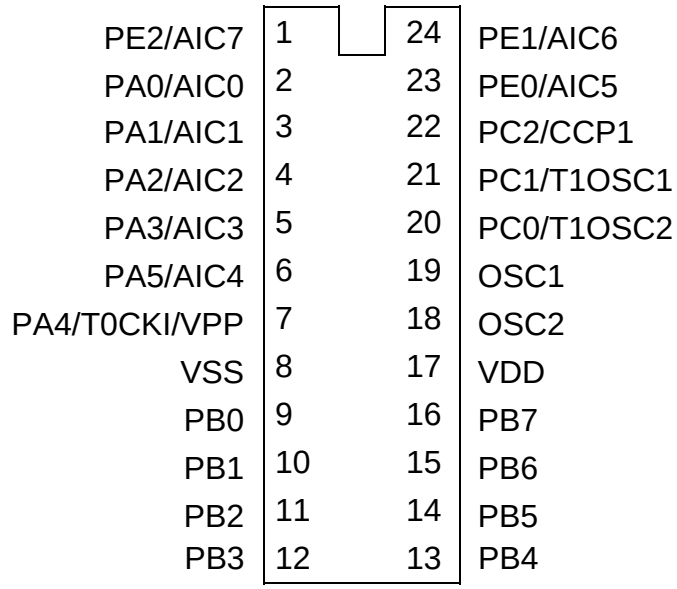
3. Applications

The application areas of this MDT10P7212 range from appliance motor control and high speed auto-motive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment



MDT10P7212K11 (SKINNY)
MDT10P7212S11 (SOP)



MDT10P7212K12 (SKINNY)
MDT10P7212S12 (SOP)

5. Order information

Device	ROM (words)	RAM (bytes)	I/O	A/D (10 bits)	Timer (8/16)	CCP	INRC (8Mhz)	Package
MDT10P7212K11	4K	192	22	8-channel	2/1	1	Yes	SKINNY
MDT10P7212S11	4K	192	22	8-channel	2/1	1	Yes	SOP
MDT10P7212K12	4K	192	20	8-channel	2/1	1	No	SKINNY
MDT10P7212S12	4K	192	20	8-channel	2/1	1	No	SOP

6. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3, PA5	I/O	Port A, TTL input level Analog input channel
PA4/T0CKI/VPP	I/O	Real Time Clock/Counter, Schmitt Trigger input levels Open drain output, Vpp input when programming
PB0~PB7	I/O	Port B, TTL input level/PB0: External interrupt input, PB4~PB7: Interrupt on pin change
PC0~PC2	I/O	Port C, Schmitt Trigger input levels
OSC1/PC4	I, I/O	Oscillator Input/external clock input PC4 in IRC mode

Pin Name	I/O	Function Description
OSC2/PC3	O, I/O	Oscillator Output/in RC mode, the CLKOUT pin has 1/4 frequency of CLKIN PC3 in IRC mode
PE0~PE2	I/O	Port E, Schmitt Trigger input levels Analog input channel
VDD		Power supply
VSS		Ground

7. Memory Map

(A) Register Map

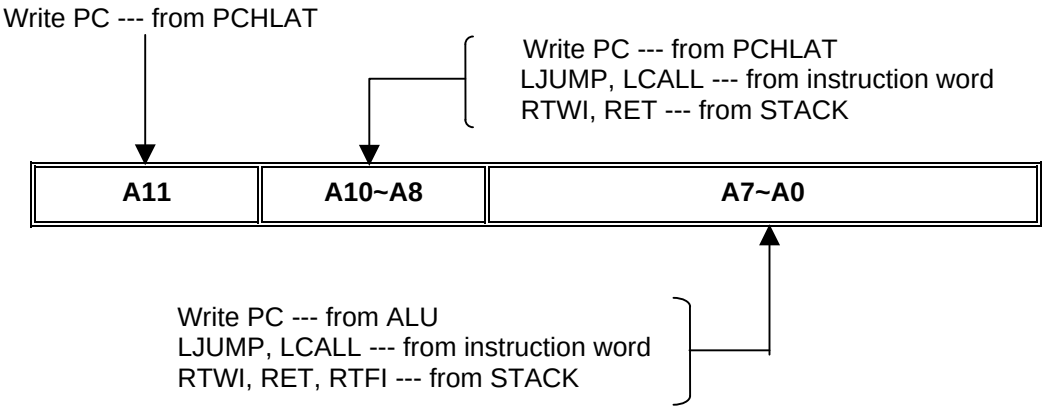
Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
07	Port C
09	Port E
0A	PCHLAT
0B	INTS
0C	PIFB1
0E	TMR1L
0F	TMR1H
10	T1STA
11	TMR2
12	T2STA
15	CCP1L
16	CCP1H

Address	Description
17	CCP1CTL
1E	ADRESH, The ADRESH register is not a writable register.
1F	ADS0
20~7F	General purpose register
BANK1	
01	TMR
05	CPIO A
06	CPIO B
07	CPIO C
09	CPIO E
0C	PIEB1
0D	PIEB2
0E	PSTA
12	T2PER
1E	ADRESL, The ADRESL register is not a writable register.
1F	ADS1
A0~FF	General purpose register

(1) IAR (Indirect Address Register): R00

(2) RTCC (Real Time Counter/Counter Register): R01

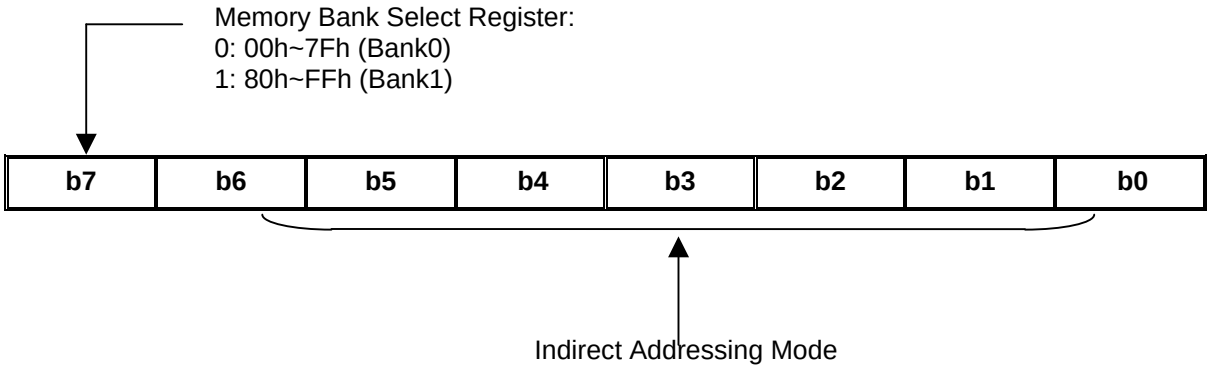
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power down Flag bit
4	/TF	WDT Timer overflow Flag bit
5	RBS0	Register Bank Select bit 0: 00h~7Fh (Bank0) 1: 80h~FFh (Bank1)
7-6	--	General purpose bit

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05
PA5~PA0, I/O Register

(7) PORT B: R06
PB7~PB0, I/O Register

(8) PORT C: R07
PC4~PC0, I/O Register

(9) PORT E: R09
PE2~PE0, I/O Register

(10) PCHLAT: R0A

(11) INTS (Interrupt Status Register): R0B

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag, Set when PB <7:4> inputs change
1	INTF	Set when INT interrupt occurs
2	TIF	Set when TMR0 overflows

Bit	Symbol	Function
3	RBIE	0: Disable PB change interrupt 1: Enable PB change interrupt
4	INTS	0: Disable INT interrupt 1: Enable INT interrupt
5	TIS	0: Disable TMR0 interrupt 1: Enable TMR0 interrupt
6	PEIE	0: Disable all peripheral interrupt 1: Enable all peripheral interrupt
7	GIS	0: Disable global interrupt 1: Enable global interrupt

(12) PIFB1 (Peripheral Interrupt Flag Bit): R0C

Bit	Symbol	Function
0	TMR1IF	TMR1 interrupt flag 0: TMR1 did not overflow 1: TMR1 overflowed
1	TMR2IF	TMR2 interrupt flag 0: No TMR2 to T2PER match occurred 1: TMR2 to T2PER match occurred
2	CCP1IF	CCP1 interrupt flag 0: No TMR1 capture/compare occurred 1: A TMR1 capture/compare occurred
5~3	--	Unimplemented, read as '0'
6	ADIF	A/D interrupt flag 0: A/D conversion is not complete 1: A/D conversion completed
7	--	Unimplemented, read as '0'

(13) TMR1L: R0E

The LSB of the 16-bit TMR1

(14) TMR1H: R0F

The MSB of the 16-bit TMR1

(15) T1STA: R10

Bit	Symbol	Function
0	TMR1ON	0: Stop TMR1 1: Enable TMR1
1	TMR1CLK	0: Internal clock (Fosc/4) 1: External clock from pin PC0
2	/T1SYNC	TMR1CLK = 1 0: Synchronize external clock 1: Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	0: TMR1 Oscillator is shut off 1: TMR1 Oscillator is enable
5~4	T1CKPS1 ~ T1CKPS0	1 1 = 1:8 Prescale value 1 0 = 1:4 Prescale value 0 1 = 1:2 Prescale value 0 0 = 1:1 Prescale value
7~6	--	Unimplemented, read as '0'

(16) TMR2: R11

TMR2 register

(17) T2STA: R12

Bit	Symbol	Function
1~0	T2CKPS1 ~ T2CKPS0	0 0 = Prescaler is 1 0 1 = Prescaler is 4 1 x = Prescaler is 16
2	TMR2ON	0: TMR2 is off 1: TMR2 is on
7~3	--	Unimplemented, read as '0'

(18) CCP1L: R15

Capture/Compare/PWM LSB

(19) CCP1H: R16

Capture/Compare/PWM MSB

(20) CCP1CTL: R17

Bit	Symbol	Function
3~0	CCP1M3 ~ CCP1M0	0 0 0 0: CCP1 off 0 1 0 0: Capture1 mode, every falling edge 0 1 0 1: Capture1 mode, every rising edge 0 1 1 0: Capture1 mode, every 4th rising edge 0 1 1 1: Capture1 mode, every 16th rising edge 1 0 0 0: Compare1 mode, set output on match 1 0 0 1: Compare1 mode, clear output on match 1 0 1 0: Compare1 mode, generate software interrupt on match 1 0 1 1: Compare1 mode, trigger special event 1 1 x x: PWM1 mode
5~4	PWM1LSB	These bits are the two LSBs of the PWM1 duty cycle
7~6	--	Unimplemented, read as '0'

(21) ADRESH: R1E

A/D result register high byte, The ADRESH register is not a writable register.

(22) ADS0 (A/D Status Register): R1F

Bit	Symbol	Function
0	ADRUN	0: A/D converter module is shut off and consumes no operating current 1: A/D converter module is operating
1	--	Unimplemented, read as '0'
2	GO/DONEB	0: A/D conversion not in progress 1: A/D conversion in progress
5~3	CHS2~0	000: AIC0 001: AIC1 010: AIC2 011: AIC3 100: AIC4 101: AIC5 110: AIC6 111: AIC7
7~6	ASCS1~0	00: fosc/2 01: fosc/8 10: fosc/32 11: f RC (*Note)

*Note: determined by OSC mode, HF: fosc/32, XT: fosc/8, RC: fosc/2, LF: fosc/2

(23) TMR (Time Mode Register): R81

Bit	Symbol	Function		
2~0	PS2~0	Prescaler Value	RTCC rate	WDT rate
		0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit 0: RTCC 1: Watchdog Timer		
4	TCE	RTCC signal edge 0: Increment on low-to-high transition on RTCC pin 1: Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set 0: Internal instruction cycle clock 1: Transition on RTCC pin		
6	IES	Interrupt edge select 0: Interrupt on falling edge on PB0 1: Interrupt on rising edge on PB0		
7	PBPH	PORTB7~0 pull-hi 0: PORTB7~0 pull-hi are enable 1: PORTB7~0 pull-hi are disable		

(24) CPIO A (Control Port I/O Mode Register): R85
＝“0”, I/O pin in output mode
＝“1”, I/O pin in input mode

(25) CPIO B (Control Port I/O Mode Register): R86
＝“0”, I/O pin in output mode
＝“1”, I/O pin in input mode

(26) CPIO C (Control Port I/O Mode Register): R87
＝“0”, I/O pin in output mode
＝“1”, I/O pin in input mode

(27) PIEB1: R8C

Bit	Symbol	Function
0	TMR1IE	TMR1 interrupt enable bit 0: Disable TMR1 interrupt 1: Enable TMR1 interrupt
1	TMR2IE	TMR2 interrupt enable bit 0: Disable TMR2 interrupt 1: Enable TMR2 interrupt
2	CCP1IE	CCP1 interrupt enable bit 0: Disable CCP1 interrupt 1: Enable CCP1 interrupt
5~3	--	Unimplemented, read as '0'
6	ADIE	A/D interrupt enable bit 0: Disable A/D interrupt 1: Enable A/D interrupt
7	--	Unimplemented, read as '0'

(28) PSTA: R8E

Bit	Symbol	Function
0	PRDB	0: Power range-detector Reset occurred 1: No Power range-detector Reset Occurred
1	PORB	0: Power on Reset occurred 1: No Power on Reset occurred
7~2	--	Unimplemented, read as '0'

(29) T2PER: R92
Timer2 period

(30) ADRESL: R9E
A/D result register low byte, The ADRESL register is not a writable register.

(31) ADS1 (A/D Status Register): R9F

Bit	Symbol	Function
2~0	PAVM2~0	0 0 0: PA0~3, PA5, PE0~2 = analog input, VREF = VDD 0 0 1: PA0~2, PA5, PE0~2 = analog input, VREF = PA3 0 1 0: PA0~3, PA5 = analog input, PE0~2 = digital I/O, VREF = VDD 0 1 1: PA0~2, PA5 = analog input, PE0~2 = digital I/O, VREF = PA3 1 0 0: PA0, 1, 3 = analog input, PA2, 5, PE0~2 = digital I/O, VREF = VDD 1 0 1: PA0, 1 = analog input, PA2, 5, PE0~2 = digital I/O, VREF = PA3 1 1 x: PA0~3, 5, PE0~2 = digital I/O
6~3	--	Unimplemented, read as '0'

Bit	Symbol	Function
7	ADFM	A/D result format select 0: Left justified, bit 5~0 of ADRESL are read as "0" 1: Right justified, bit 7~2 of ADRESH are read as "0"

(32) Configurable options for EPROM (Set by writer)

Oscillator Type
RC Oscillator
HFXT Oscillator
XTAL Oscillator
LFXT Oscillator

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-range control
Power-range disable
Power-range enable

Oscillator-start Timer control
0ms
75ms

Power-edge Detect
PED Disable
PED Enable

Security state
Security Disable
Security Enable

(B) Program Memory

Address	Description
000-FFF	Program memory
000	The starting address of power on, external reset or WDT time-out reset
004	Interrupt vector

8. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	0Ah,02h	0000 0000 0000	0000 0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah	---0 0000	---0 0000	---u uuuu
INTS	0Bh	0000 000x	0000 000u	uuuu uuuu
PIFB1	0Ch	-000 0000	-000 0000	-uuu uuuu
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1STA	10h	--00 0000	--uu uuuu	--uu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2STA	12h	---- -000	---- -uuu	---- -uuu
CCP1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CTL	17h	--00 0000	--00 0000	--uu uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS0	1Fh	0000 00-0	0000 00-0	uuuu uu-u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	--11 1111	--11 1111	--uu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	1111 1111	1111 1111	uuuu uuuu
PIEB1	8Ch	-000 0000	-000 0000	-uuu uuuu
PSTA	8Eh	---- --0u	---- --uu	---- --uu
T2PER	92h	1111 1111	1111 1111	1111 1111
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS1	9Fh	0--- -000	0--- -000	u--- -uuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3	PSTA: bit 1	PSTA: bit 0
WDT reset (not during SLEEP)	0	1	u	u
WDT reset during SLEEP	0	0	u	u
Power-on reset	1	1	0	x
Power-range reset	1	1	u	0

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

9. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return from subroutine	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R － W→t or (R+/W+1 →t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R － 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R － 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C

Instruction Code	Mnemonic Operands	Function	Operating	Status
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI i	Add immediate to W	W+i→W	C,HC,Z
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI i	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Reture from interrupt	Stack→PC,1→GIS	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address